STD95NH02L-1
STD95NH02L

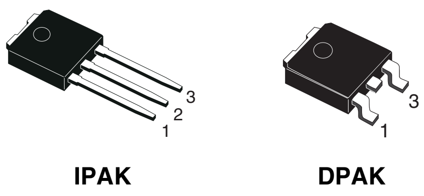
N-channel 24V - 0.0039Ω - 80A - DPAK - IPAK
Ultra low gate charge STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STD95NH02L	24V	< 0.005Ω	80A(1)
STD95NH02L-1	24V	< 0.005Ω	80A(1)

1. Value limited by wire bonding

- Conduction losses reduced
- Switching losses reduced
- Low threshold device



Description

The device is based on the latest generation of ST's proprietary STripFET™ technology. An innovative layout enables the device to also exhibit extremely low gate charge for the most demanding requirements in high-frequency DC-DC converters. It's therefore ideal for high-density converters in Telecom and Computer applications.

Application

- Switching applications

Figure 1. Internal schematic diagram

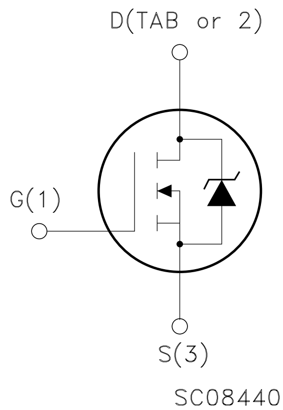


Table 1. Device summary

Order code	Marking	Package	Packaging
STD95NH02LT4	D95NH02L	DPAK	Tape & reel
STD95NH02L-1	D95NH02L	IPAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{spike} (1)	Drain-source voltage rating	30	V
V_{DS}	Drain-source voltage (V_{GS} = 0)	24	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20kΩ)	24	V
V_{GS}	Gate-source voltage	± 20	V
I_D (2)	Drain current (continuous) at T_C = 25°C	80	A
I_D (2)	Drain current (continuous) at T_C = 100°C	68	A
I_{DM} (3)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25°C	100	W
	Derating factor	0.67	W/°C
E_{AS} (4)	Single pulse avalanche energy	600	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Guaranteed when external Rg= 4.7Ω and Tf < Tfmax
2. Value limited by wire bonding
3. Pulse width limited by safe operating area
4. Starting Tj =25°C, Id = 40A, Vdd = 22V

Table 3. Thermal data

Rthj-case	Thermal resistance junction-case max	1.5	°C/W
Rthj-amb	Thermal resistance junction-to ambient max	100	°C/W
T_J	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} =0	24			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 20V V_{DS} = 20V, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 40A V_{GS} = 5V, I_D = 40A		0.0039 0.0055	0.005 0.009	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 10V, I_D = 10A		30		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 15V, f = 1MHz, V_{GS} = 0		2070 990 90		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 12V, I_D = 40A R_G = 4.7Ω V_{GS} = 10V (see *Figure 14*)		20 110 47 20		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 12V, I_D = 80A, V_{GS} = 5V, R_G = 4.7Ω (see *Figure 15*)		17 7.6 6.8		nC nC nC
Q_{oss} (2)	Output charge	V_{DS} =19V, V_{GS} =0V		22.6		nC
Q_{gls} (3)	Third-quadrant gate charge	V_{DS} < 0V, V_{GS} = 5V		15		nC
R_G	Gate Input Resistance	f=1MHz Gate DC Bias =0 Test Signal Level =20mV Open Drain		1.8		Ω

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.
2. $Q_{oss.} = C_{oss} * \Delta$ Vin, $C_{oss} = C_{gd} + C_{gd.}$ See *Chapter 4: Appendix A*
3. Gate charge for synchronous operation

Table 6. **Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				80 320	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 40A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 80A, di/dt = 100A/µs, V_{DD} = 20V, T_j = 150°C (see *Figure 16*)		42 50.4 2.4		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

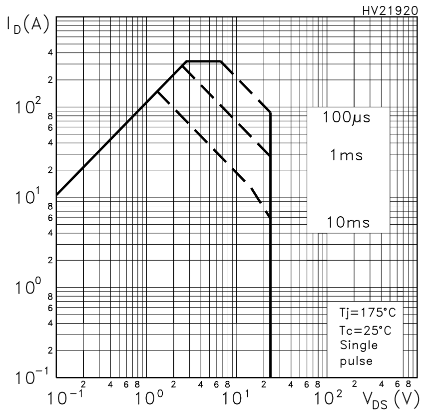


Figure 3. Thermal impedance

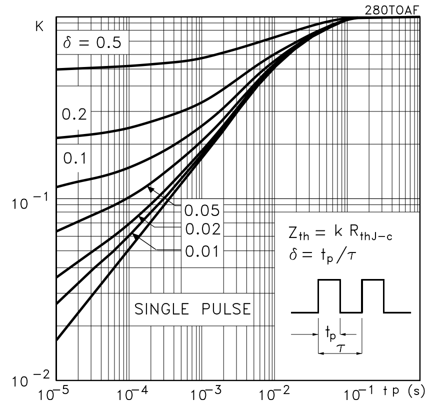


Figure 4. Output characteristics

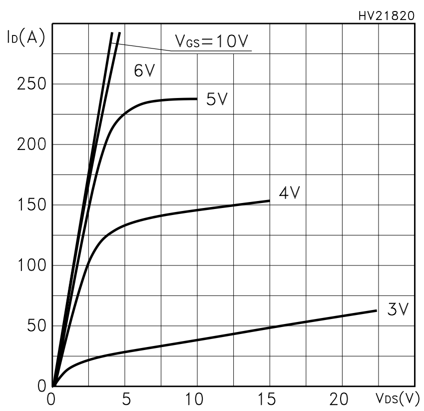


Figure 5. Transfer characteristics

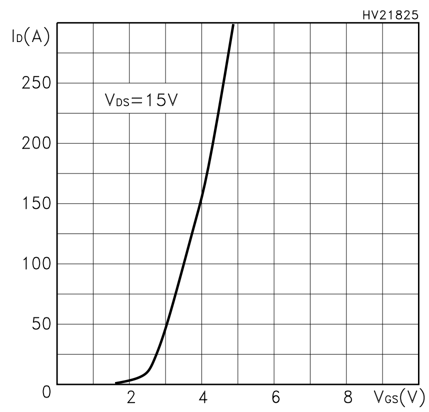


Figure 6. Transconductance

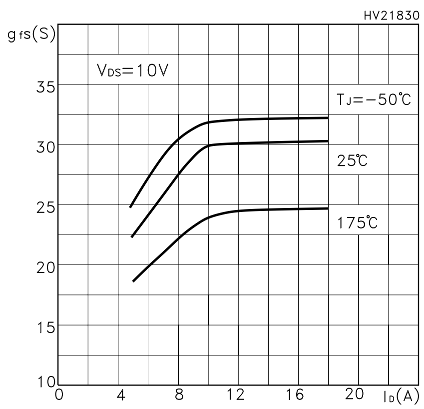


Figure 7. Static drain-source on resistance

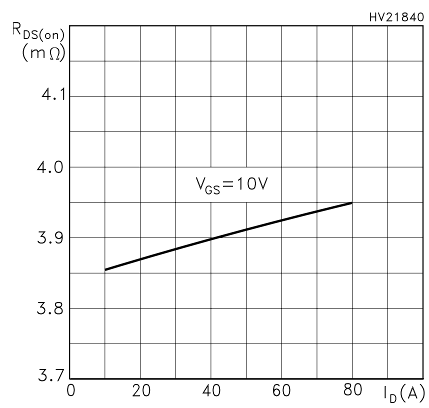


Figure 8. Gate charge vs gate-source voltage

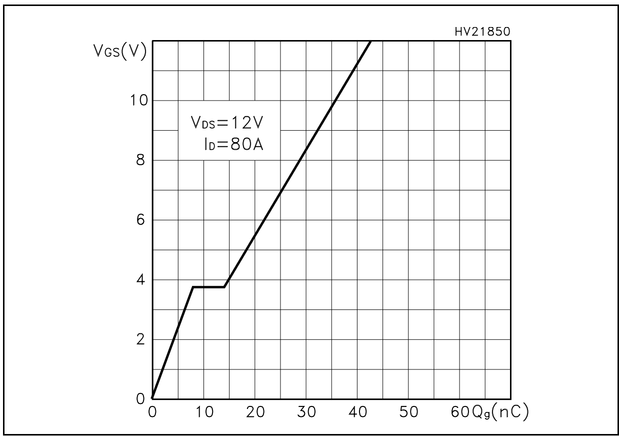


Figure 9. Capacitance variations

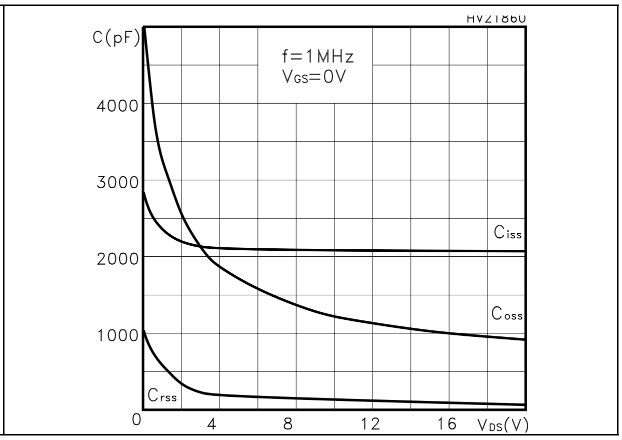


Figure 10. Normalized gate threshold voltage vs temperature

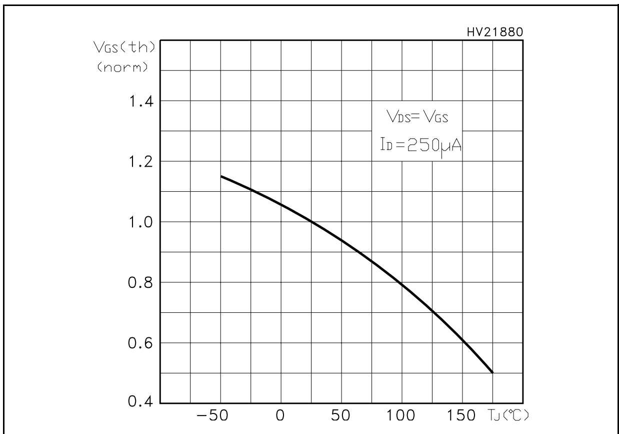


Figure 11. Normalized on resistance vs temperature

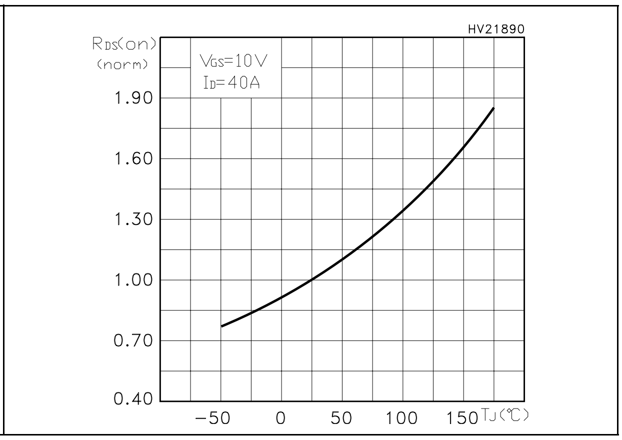


Figure 12. Source-drain diode forward characteristics

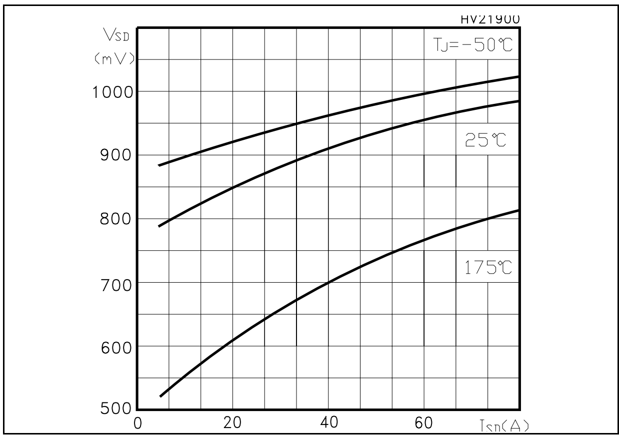
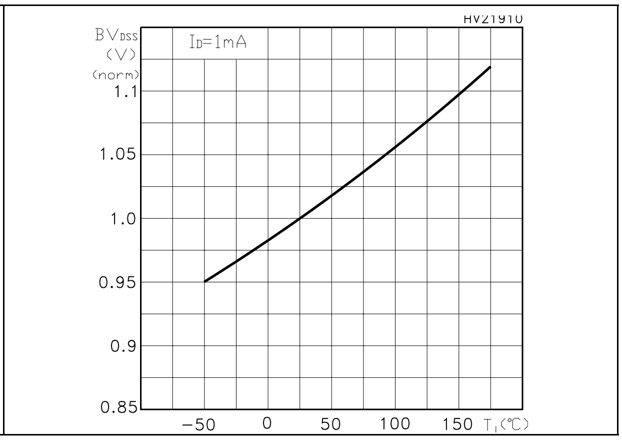


Figure 13. Normalized BV_{DSS} vs temperature



3 Test circuit

Figure 14. Switching times test circuit for resistive load

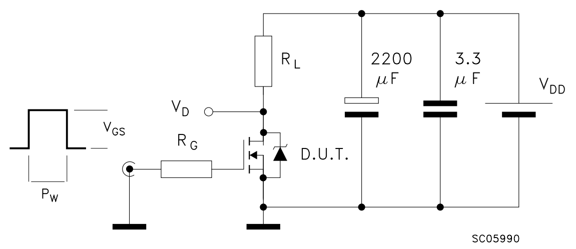


Figure 15. Gate charge test circuit

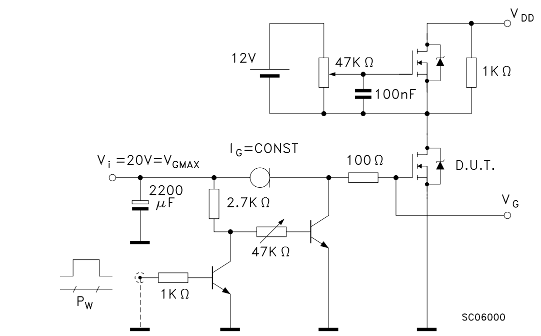


Figure 16. Test circuit for inductive load switching and diode recovery times

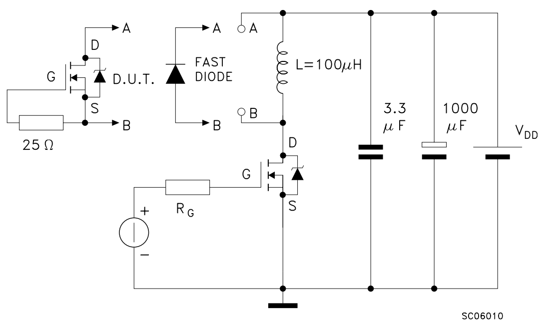


Figure 17. Unclamped Inductive load test circuit

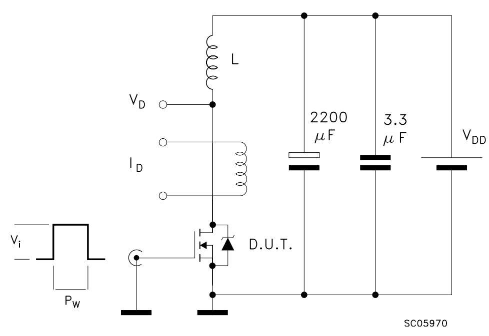


Figure 18. Unclamped inductive waveform

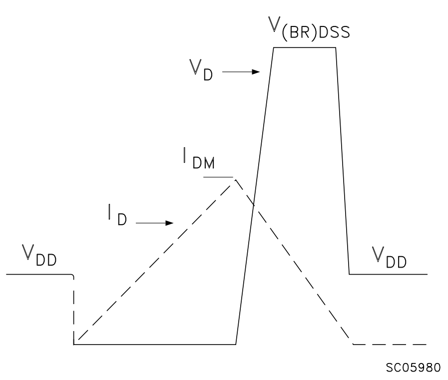
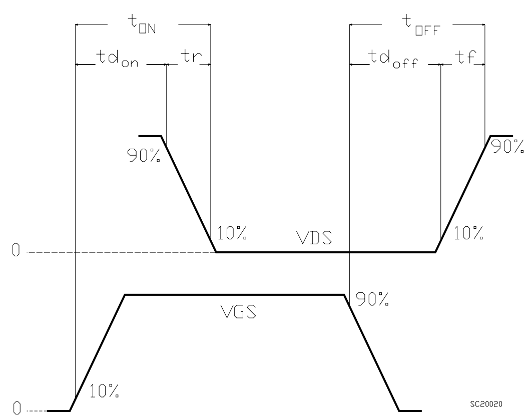
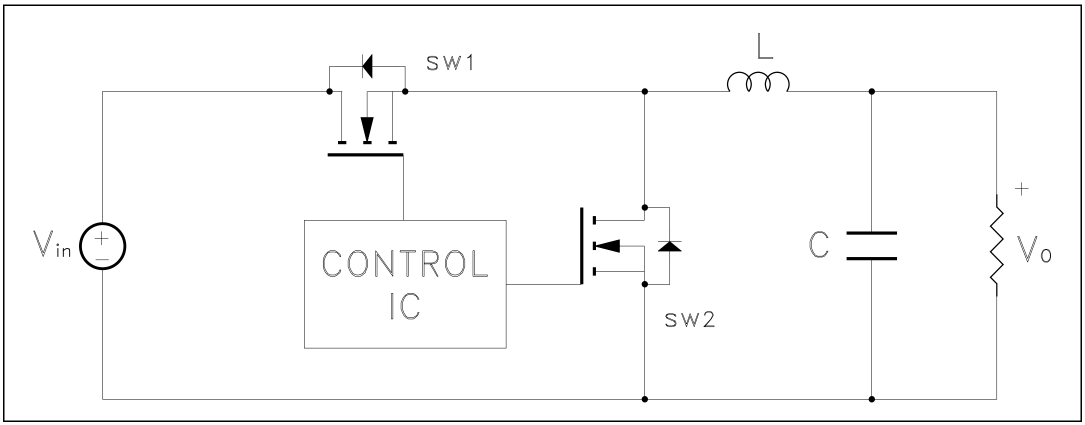


Figure 19. Switching time waveform



4 Appendix A

Figure 20. Buck converter: power losses estimation



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Qgls to reduce the gate charge losses
- Small Coss to reduce losses due to output capacitance
- Small Qrr to reduce losses on SW1 during its turn-on
- The Cgd/Cgs ratio lower than Vth/Vgg ratio especially with low drain to source
- voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
- Small Rg and Ls to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Qg to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

Table 7. Power losses calculation

	High side switching (SW1)	**Low side switch (SW2)**
Pconduction	$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1-\delta)$
Pswitching	$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching

Table 7. Power losses calculation

		High side switching (SW1)	Low side switch (SW2)
Pdiode	Recovery (1)	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
Pgate(Q_G)		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P_{Qoss}		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

Table 8. Parameters meaning

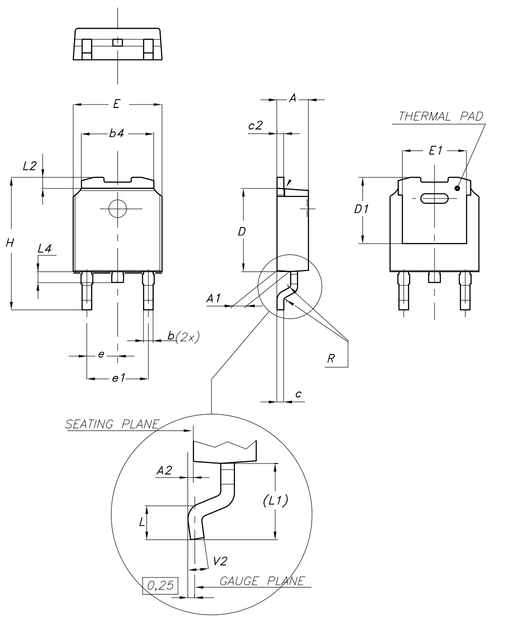
Parameter	Meaning
d	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P_{Qoss}	Output capacitance losses

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

DPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



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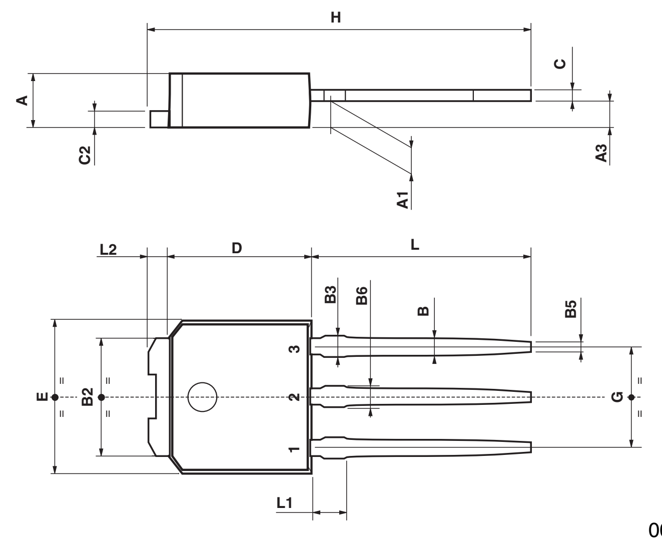
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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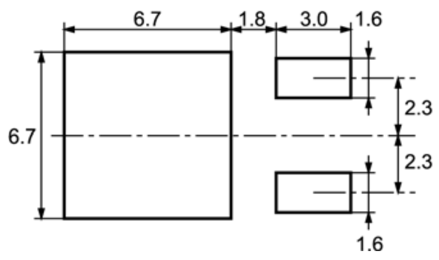
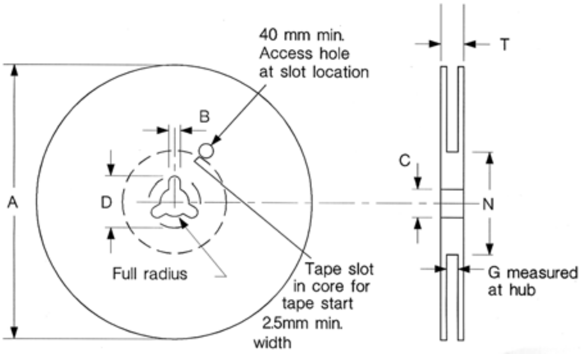
6 Packing mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



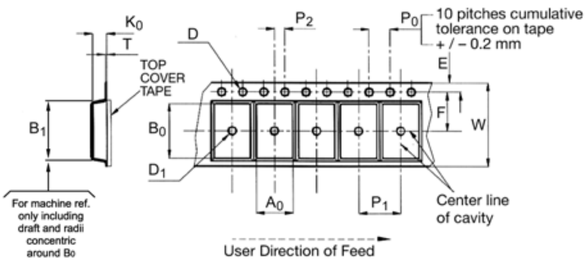
REEL MECHANICAL DATA

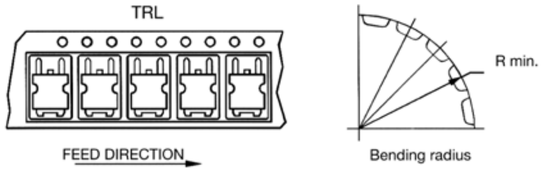
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641





7 Revision history

Table 9. Revision history

Date	Revision	Changes
13-Sep-2004	1	First release
27-May-2005	2	Some values changed in *Table 5: Dynamic*.
09-Aug-2006	3	The document has been updated
02-Aug-2007	4	Error on cover page; added IPAK